AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

Claims 1-10 (Canceled)

11. (Currently amended) A circuit comprising:

a first signal generation circuit for generating [[an]] a first output signal having a frequency which is proportional to that of [[an]] a first input signal, said first signal generation circuit comprising

a first phase locked loop (PLL) circuit for generating [[an]] a first intermediate signal having a frequency which is proportional to the first input signal frequency; and

a second phase locked loop circuit for generating the first output signal having a frequency which is proportional to the first intermediate signal frequency;

wherein, for a given first input signal frequency and a given first output signal frequency, the first intermediate signal frequency is selectable from a first plurality of available frequencies;

a second signal generation circuit for generating a second output signal having a frequency which is proportional to that of a second input signal, said second signal generation circuit comprising

a third phase locked loop circuit for generating a second intermediate signal having a frequency which is proportional to the second input signal frequency; and

a fourth phase locked loop circuit for generating the second output signal having a frequency which is proportional to the second intermediate signal frequency;

wherein the first input signal frequency is substantially identical to the second input signal frequency; and

wherein the first and second signal generation circuits are configured so that the first output signal frequency is substantially identical to the second output signal

frequency, but also configured so that the first intermediate signal frequency is different than the second intermediate signal frequency.

12. (Original) The circuit of claim 11 wherein the first PLL has a lower bandwidth than the second PLL.

13. (Currently amended) The circuit of claim 11 wherein the first input signal is derived from a reference signal for a serial data signal.

14. (Currently amended) The circuit of claim 12 wherein the bandwidth of the first PLL is selectable from a first plurality of values.

15. (Currently amended) The circuit of claim 11 wherein the first output signal frequency is equal to M times the first input signal frequency, where M is a positive integer.

16. (Currently amended) The circuit of claim 11 wherein the first output signal frequency is equal to M/N times the first input signal frequency, where M and N are both positive integers.

17. (Currently amended) The circuit of claim 11 wherein the first output signal frequency is other than an integer ratio times the first input signal frequency.

18. (Currently amended) The circuit of claim 11 wherein each of the first plurality of available frequencies falls by at least a predetermined offset from any harmonic frequency of the given first input signal frequency and the given first output signal frequency.

19. (Currently amended) The circuit of claim 18 wherein the first plurality of available frequencies numbers at least five.

20. (Currently amended) The circuit of claim 18 wherein the first plurality of available frequencies are spaced approximately 2.5% apart, relative to a nominal first intermediate signal frequency.

21. (Currently amended) The circuit of claim 18 wherein the first plurality of available frequencies are spaced approximately 1.25% apart, relative to a nominal first intermediate signal frequency.

22. (Original) The circuit of claim 11 encoded in a computer readable medium suitable for design, test, or manufacture of an integrated circuit.

23. (Currently amended) The circuit of claim 11 ~~further comprising:~~

~~a second signal generation circuit for generating a second output signal having a frequency which is proportional to that of a second input signal, said second signal generation circuit comprising~~

~~a third phase locked loop (PLL) circuit for generating a second intermediate signal having a frequency which is proportional to the second input signal frequency; and~~

~~a fourth phase locked loop circuit for generating the second output signal having a frequency which is proportional to the second intermediate signal frequency;~~

wherein, for a given second input signal frequency and a given second output signal frequency, the second intermediate signal frequency is selectable from a second plurality of available frequencies.

24. (Original) The circuit of claim 23 wherein the first and second signal generation circuits are substantially identical.

25. (Currently amended) The circuit of claim [[23]] 11 wherein the first and second signal generation circuits are disposed within a single integrated circuit.

26. (Currently amended) The circuit of claim [[23]] 11 wherein the first and second signal generation circuits are disposed within different integrated circuits on a single printed wiring board.

27. (Currently amended) The circuit of claim [[23]] 11 wherein the first and second signal generation circuits are disposed on different printed wiring boards within one system enclosure.

28. (Currently amended) The circuit of claim [[23]] 11 wherein the first and second input signals are ~~nominally identical in frequency, but~~ associated with independent serial data channels.

Claims 29-32 (Canceled)

33. (Currently amended) A method comprising:

generating a first intermediate signal having a frequency which is a first factor times a first input signal frequency;

generating a first output signal having a frequency which is a second factor times the first intermediate signal frequency;

choosing the first intermediate signal frequency from a plurality of available frequencies by appropriately choosing the first factor; ~~and~~

choosing the second factor to result in a desired proportionality between the first input signal and the first output signal;

generating a second intermediate signal having a frequency which is a third factor times a second input signal frequency;

generating a second output signal having a frequency which is a fourth factor times the second intermediate signal frequency;

choosing the second intermediate signal frequency from a second plurality of available frequencies by appropriately choosing the third factor; and

choosing the fourth factor to result in a desired proportionality between the second input signal and the second output signal;

wherein the first input signal frequency is substantially identical to the second input signal frequency;

wherein the first output signal frequency is substantially identical to the second output signal frequency; and

wherein the first intermediate signal frequency is different than the second intermediate signal frequency.

34. (Original) The method of claim 33 further comprising using a first phase-locked loop circuit to generate the first intermediate signal.

35. (Original) The method of claim 33 further comprising using a second phase-locked loop circuit to generate the first output signal.

36. (Original) The method of claim 35 further comprising configuring the first phase-locked loop circuit with a lower bandwidth than the second phase-locked loop circuit.

37. (Original) The method of claim 33 further comprising choosing the first intermediate signal frequency to avoid harmonics of the first input signal and the first output signal.

38. (Canceled)

39. (Currently amended) The method of claim [[38]] 33 further comprising generating the first and second output signals within a single integrated circuit.

40. (Currently amended) The method of claim [[38]] 33 further comprising generating the first and second output signals on a single printed wiring board.

41. (Currently amended) The method of claim [[38]] 33 further comprising generating the first and second output signals on different printed wiring boards within one system enclosure.

42. (Canceled)

43. (Currently amended) The circuit of claim [[23]] 11 wherein the first and second signal generation circuits each comprises a clock multiplying circuit.

44. (Previously presented) The circuit of claim 43 wherein the first and second signal generation circuits each comprises a portion of a serial digital communications circuit.

45. (New) The method of claim 33 wherein the first and second input signals are associated with independent serial channels.

46. (New) The circuit of claim 12 wherein the third PLL has a lower bandwidth than the fourth PLL.

47. (New) The circuit of claim 28 wherein the first and second input signals are derived from a respective reference signal for a respective serial data signal.

48. (New) The circuit of claim 23 wherein the respective bandwidth of the first PLL and the third PLL is selectable from a respective plurality of values.

49. (New) The circuit of claim 23 wherein each of the first and second pluralities of available frequencies falls by at least a predetermined offset from any harmonic frequency of the given first input signal frequency and the given first output signal frequency.

50. (New) The circuit of claim 49 wherein the first and second plurality of available frequencies each numbers at least five.